REMARKS

This application has been carefully reviewed in view of the current Office Action in which U.S. Patent Publication 2001/0052786 to Eldridge et al. (Eldridge hereinafter) was cited as anticipating all of claims 23-33 and all claims were also rejected as indefinite. Claims 1-22 were cancelled in view of their prosecution in the parent application, now U.S. Patent No. 6,645,841.

Regarding the Indefiniteness Rejection

The Office Action indicates that claims 23-33 are indefinite due to uncertainty in the meaning of the language "by virtue of omission of a solder bump". While Applicant felt that this language was clear, claim 23 has been amended to add clarifying language that explains that *"at least one block of circuitry can be selectively configured by selectively making an electrical connection between the substrate and the integrated circuit die, the block of circuitry to be selectively configured having at least one solder pad that is used to selectively connect to the block of circuitry in order to configure the block of circuitry"*. This language, together with minor changes to the last sub-paragraph of the claim, indicates that "configuration" is carried out by omission of a solder bump. The language is believed to clearly and distinctly claim the present embodiment using language that is similar to that which was found acceptable in the parent application, claim 17. Moreover, the meaning of "configure" and similar terms is clearly explained in the specification, for example at pages 8 and 9. Accordingly, the claims as amended are believed clear and of the same scope as originally presented. Reconsideration and allowance is respectfully requested.

Regarding the Anticipation Rejection Based on Eldridge

The Examiner cites in particular, Figs. 1, 3A, 6 and 9, along with paragraphs 49, 55, 58 and 70, of the Eldridge et al. reference in support of this rejection. Applicant has reviewed these portions of the reference in particular, along with the entire reference as a whole and respectfully traverses the rejection as follows:

The Eldridge publication shows use of "special contact pads 112" (or 412 or 612) that are situated on the surface of an integrated circuit along with bond pads 110 (or 410 or 610). These "special contact pads" are used to access circuitry for testing that would not normally be accessible through use of the bond pads 110. While it is clear that certain bond pads 110, might be used only for testing, it is equally clear that the "special contact pads" 112 are not intended to be used for soldering pads (or for wirebonding for that matter). These "special contact pads" 112 are only used for probing the chip to determine if there are defects or to apply test signals. The undersigned presumes that the fact that these special contact pads 112 are not actually bonded may be the source of the Examiner's interpretation of Eldridge leading to the rejections, as was the case in the parent application.

Applicant's invention, on the other hand, in certain embodiments thereof, uses multiple arrangements of solder pads that can be used to connect to the integrated circuit chip in multiple ways. One simple example that should not be considered limiting is explained in the specification at the location noted above which states *"By way of example, a logic gate input having a pull-up resistor can be selectively connected to ground to provide a hard wired logic signal input to a logic circuit by selectively either providing or omitting a solder bump to make the connection from the gate's input to ground."* Thus, by selectively omitting a solder bump, a block of circuitry can be configured. While paragraph 70 of Eldrige et al. does in fact disclose that an enable signal or clock signal can be provided to the circuitry using a "special contact pad", this must be taken in the context of paragraphs 47-51 of the reference which explain that these pads are in fact simply used as probe pads for testing purposes. The undersigned has reviewed Eldridge et al. and finds no teaching or suggestion, either in the passages cited by the Examiner or elsewhere that would suggest otherwise.

With reference to independent claim 23, it is noted that this claim calls for selective omission of a connection between a solder bump to a solder pad. The undersigned notes that in order to use a solder bump to connect to the circuitry, a solder pad is needed on the chip to bond therewith. If it is a solder pad, it is not a "special contact pad" within the meaning of Eldridge. By implication, the excluded circuitry

clearly has solder pads that are not soldered in order to conform to the language of claim 23. Since there is no disclosure in Eldridge of configuring circuitry in a chip by selective omission or application of solder bumps as claimed, there can be no anticipation. Accordingly, reconsideration and allowance of claim 23 is respectfully requested.

With regard to claims 24-33, these claims are dependent upon allowable claim 23 and thus are also believed allowable. Although further distinctions exist in these claims, discussions of such differences are believed moot in view of the above discussion of claim 23. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action. Reconsideration and allowance is respectfully requested.

In view of this communication, all claims are now believed to be in condition for allowance and such is respectfully requested at an early date.

Respectfully submitted,

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